REMARKS

In accordance with the foregoing, claims 1-4 have been amended and claim 5 is cancelled. No new matter is presented and, accordingly, approval and entry of the foregoing amended claims are respectfully requested.

STATUS OF CLAIMS

Claims 1-5 are rejected.

Claim 3 is objected to but is indicated to be allowable if suitably rewritten to be dependent upon a rejected base claim or if rewritten to independent form including all the limitations of the respective base and any intervening claims. In the foregoing, claim 3 has been amended to independent form, incorporating the limitations of claim 1 from which it originally depended and, accordingly, now stands as an independent claim and is submitted to be allowable.

Claim 5 is cancelled and the recitation thereof is now incorporated in claim 1. .

Claims 1-4 are pending and under consideration.

ITEM 2: REJECTION OF CLAIM 4 FOR INDEFINITENESS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Claim 4, as originally filed, inadvertently depended from claim 1 but was intended to depend from claim 3, which provides antecedent support for the limitation "the address acknowledge signal" in line 4 of claim 4. In the foregoing, claim 4 is now amended to depend from claim 3, thereby overcoming the indefiniteness.

The oversight is regretted.

The Examiner's statement in the Action in Item 2, to the effect that the Examiner assumed that "Applicant means <u>any type of acknowledge signal</u>" is respectfully submitted to be in error. (Emphasis added). This greatly impacts the prior art rejections of Items 6-10, addressed below.

Moreover, the rejection of claim 4 in Item 9 at page 5 of the Action, appears to have been based on that incorrect, broadened interpretation of "acknowledge signal:"

> Per claim 4, Hatae combined with Ooi discloses claim 1, wherein the data send unit initiates transmission of predetermined units of data stored in the send/receive buffer (Fig. 4, element 114, DMA START initiates transfer), after an interrupt to the CPU generated when the acknowledge detection unit detects an <u>acknowledge signal</u> (Fig. 4, element 113, DMA start signal received at the bus controller, element 26).

(Action at page 5; emphasis added).

ITEMS 6-10: REJECTION OF CLAIMS 1 AND 2-5 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER HATAE ET AL. (U.S. PATENT 5,724,609) IN VIEW OF OOI ET AL. (U.S. PUBLICATION NO. 2003/0005231)

The rejections are respectfully traversed.

Independent claims 1 and 3 have been amended in the foregoing to clarify "the data send unit repeats the next data transmission with the predetermined unit of data, in response to detection of the data acknowledge signal by the acknowledge detection unit, without generating any interrupt to the CPU". Thus, the present invention, as claimed, relates to a serial transfer bus having a single data line and a single clock line, in which the data transfer is carried out serially over the single data line in synchronization with a clock driven onto the clock line. Further, the data send unit transmits the predetermined unit of data serially via the serial transfer bus, the receiving device generates the data acknowledge signal when receiving the predetermined unit of data, and the data send unit repeats the next data transmission with the predetermined unit of data, in response to detection of the data acknowledge signal by the acknowledge detection unit, without generating any interrupt to the CPU. Therefore, the CPU interrupt frequency can be lowered.

It is respectfully submitted that Hatae et al. does not relate to an integrated circuit device having a send/receive macro for serially transferring addresses and data to or from an external device via a serial transfer bus as defined by claim 1, does not disclose that a data send unit serially transmits the predetermined unit of data via the serial transfer bus, that the receiving device generates the data acknowledge signal when receiving the predetermined unit of data, and that the data send unit repeats the next data transmission with the predetermined unit of data, in response to detection of the data acknowledge signal by the acknowledge detection unit, without generating any interrupt to the CPU - - all as set forth in independent claim 1.

Hatae expressly teaches "an interruption acknowledge signal" throughout the specification and the same is employed as the exclusive type of acknowledge signal in the claims of the reference - - see e.g., column 12, lines 39-40, column 13, line 26, etc. - - contrary to the data acknowledge signal" processed in the integrated circuit device as claimed herein and which results in the "acknowledge detection unit generating a data acknowledge signal non-detection interrupt to the CPU...." It further follows that the Examiner's assumption that "Applicant means any type of acknowledge signal" as set forth in Item 2 (in relation to claim 4, discussed hereinabove) is in error.

At page 4 of the Action, the Examiner concedes that "Hatae does not disclose expressly the bus and external device (Fig. 1, element 44, the magnetic disk unit) being serial based. On the other hand, the Action asserts:

> Ooi discloses use of serial ATA hard device and associated serial bussing schemes...and use of DMA....

It is submitted that Ooi et al. is of a rather different character then Hatae, pointing out deficiencies of each of "parallel ATA..." (paragraph [0005]) and "Serial ATA..." (paragraph [0006]) - - and wherein Ooi purports to address the need to "have an efficient technique to emulate parallel ATA interface in a serial ATA environment." (paragraph [0007]).

It is respectfully submitted that the contention in the Item at page 4, that "Hatae and Ooi are analogous art because they are from a similar problem solving area in how to minimize interrupts to the CPU with the use of DMA, directed to data transfer to hard drive," is contrary to the clear distinctions between the teachings of the two references - - and, in any event, neither can serve to supplement the deficiencies of the other.

It is respectfully submitted that the pending claims patentably distinguish over the references, taken singularly or in any proper combination.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: June 22, 2007

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